1. (Currently Amended) A system for processing digital signals comprising symbols propagated according to a period, the system comprising:

a signal conditioning filter comprising a first stage for mitigating degradations of a digital signal that occur according to a first time scale, the first stage comprising a linear tapped-delay line filter tuned to the first time scale, the first time scale comprising a fraction of the period at which the symbols are propagated, and a second stage for removing signal distortions that occur according to a second time scale, the second stage comprising a linear tapped-delay line filter tuned to the second time scale, the second time scale being different than the first time scale and comprising a magnitude at least equal to the period at which the symbols are propagated; and

a signal integrity unit for controlling the signal conditioning filter by maximizing fidelity of the digital signals.

2. (Cancelled.)

3. (Currently Amended) The system of Claim [[2]]1, wherein the signal conditioning filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

4. (Currently Amended) The system of Claim [[2]]1, wherein [[the]]each tapped delay-line filter comprises LC circuits.

5. (Currently Amended) The system of Claim [[2]]1, wherein delays are distributed across both [[the]] input and output branches of [[the]]each tapped delay-line filter.

6. (Currently Amended) The system of Claim [[2]]1, wherein [[the]] parasitic capacitances from one of an input and output of [[the]]each tapped-delay line filter are absorbed into [[the]]an LC design circuit and are used to implement the delay.

7. (Original) The system of Claim 1, wherein the digital signals comprise binary signals.

8. (Original) The system of Claim 1, wherein the digital signals comprise multilevel signals.

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9. (Currently Amended) The system of Claim 1, wherein the first and second stages comprise various signal paths of different lengths where time delays produced by the signal paths are re-used.

10. (Currently Amended) A system for processing digital signals comprising:

a first filter stage comprising a first linear tapped-delay line filter tuned ~~operating according~~ to a first time constant, the first time constant comprising a value that is less than a symbol period, for compensating for signal distortions that occur within a single symbol period and for integrating over less than a symbol period in order to substantially reduce at least one of ringing, jitter, and noise; and

a second filter stage comprising a second linear tapped-delay line filter tuned ~~operating according~~ to a second time constant, the first time constant being smaller than the second time constant and the second time constant comprising value at least equal to a symbol period, the second filter stage for removing inter-symbol interference (ISI).

11. (Cancelled).

12. (Currently Amended) The system of Claim [[11]]10, wherein ~~the signal conditioning~~ each filter comprises a coefficient amplifier, the coefficient amplifier comprising a Gilbert cell multiplier.

13. (Currently Amended) The system of Claim [[11]]10, wherein [[the]]each tapped delay-line filter comprises LC circuits.

14. (Currently Amended) The system of Claim [[11]]10, wherein delays are distributed across both [[the]] input and output branches of [[the]]each tapped delay-line filter.

15. (Currently Amended) The system of Claim [[11]]10, wherein [[the]] parasitic capacitances from one of an input and output of [[the]]each tapped-delay line filter are absorbed into the LC design circuit and are used to implement the delay.

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16. (Currently Amended) The system of Claim [[11]]10, wherein the digital signals comprise binary signals.

17. (Currently Amended) The system of Claim [[11]]10, wherein the digital signals comprise multilevel signals.

18. (Currently Amended) The system of Claim [[11]]10, wherein the first and second filtering stages form part of a unit for receiving digital signals.

19. (Currently Amended) The system of Claim [[11]]10, wherein the first and second filtering stages form part of a unit for transmitting digital signals.

20. (Currently Amended) A system for processing digital signals comprising symbols propagated according to a period, the system comprising:

a cascade of two linear filters, where each filter comprises a series of variable gain amplifiers connected ~~between a first delay element and a second~~ by delay elements, each delay element for a respective filter having a same delay value, each linear filter equalizing a particular frequency band of a multilevel signal;

the delay elements in the first filter being tuned to a fraction of the symbol period at which the symbols are propagated for compensating for signal distortions that occur within a single symbol period and for integrating over less than a symbol period in order to substantially reduce at least one of ringing, jitter, and noise;

the delay elements in the second filter being tuned to a magnitude at least equal to the symbol period at which symbols are propagated for mitigating degradations that occur according to the period.

21. (Currently Amended) The system of Claim 20, wherein [[the]]each variable gain amplifier comprises a Gilbert Cell multiplier.

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22. (Currently Amended) The system of Claim 20, wherein the ~~first and second~~ delay elements of the first and second filters comprise delay lines.

23. (Currently Amended) The system of Claim 20, wherein the ~~first and second~~ delay elements of the first and second filters comprise delay lines that include LC circuits.

24. (Original) The system of Claim 20, further comprising a signal integrity unit for controlling each filter.

25. (Currently Amended) The system of Claim [[22]]24, wherein the signal integrity unit measures fidelity of [[the]]a filtered signal, each filter further comprising a variable gain coefficient amplifier, and gains of [[the]] each variable gain coefficient amplifier[[s]] are controlled to maximize fidelity measured by the signal integrity unit.

26. (Currently Amended) A method for monitoring and improving the fidelity of a ~~digital~~ communications signal comprising:

receiving a ~~digital~~communications signal;

applying an adjustable linear conditioning filter that compensates for signal distortions;

determining a quality of the ~~digital~~communications signal after the conditioning filter by using a low pass filter followed by an analog-to-digital converter to digitize output of the low pass filter and estimating the quality of the digital output from the analog-to-digital converter with a microcontroller;

in response to determining the quality of the received communications signal, adjusting one or more parameters of the conditioning filter with the microcontroller to improve the quality of the ~~digital~~communications signal.

27. (Currently Amended) The method of Claim 26, wherein adjusting one or more parameters of the linear conditioning filter further comprises adjusting one or more variable gain amplifiers.

28. (Original) The method of Claim 26, further comprising propagating the received signal through a series of delay lines with each delay having approximately the same delay value.

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29. (Cancelled).

30. (Currently Amended) The method of Claim [[29]]26, wherein ~~empirically calculating the estimated fidelity measure~~ the microcontroller ~~comprises~~ usinges coordinate descent to improve the quality of the communications signal.

31. (Currently Amended) The method of Claim [[29]]26, wherein ~~empirically calculating the estimated fidelity measure~~ the microcontroller ~~comprises~~ usinges a gradient descent to improve the quality of the communications signal.

32. (Currently Amended) The method of Claim [[29]]26, wherein ~~calculating an estimated fidelity measure~~ the microcontroller ~~comprises~~ determininges a regularization component to guide a solution to one or more parameters of the conditioning filter to ~~the fidelity measure to~~ a predetermined bias.

33. (New) The method of Claim 26, further comprising adjusting a reference voltage with the microcontroller via a digital-to-analog converter to generate a value of a cumulative distribution function at the output of the low pass filter.

34. (New) The method of Claim 33, further comprising analyzing the cumulative distribution function with the microcontroller to adjust the parameters of the conditioning filter.

35. (New) The method of Claim 26, further comprising processing the cumulative distribution function with the microcontroller to estimate the fidelity of the signal output from the conditioning filter.

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